Electronic Ionic Contamination Is Not Only Confined to Flux Residues - PCB Cleanliness?

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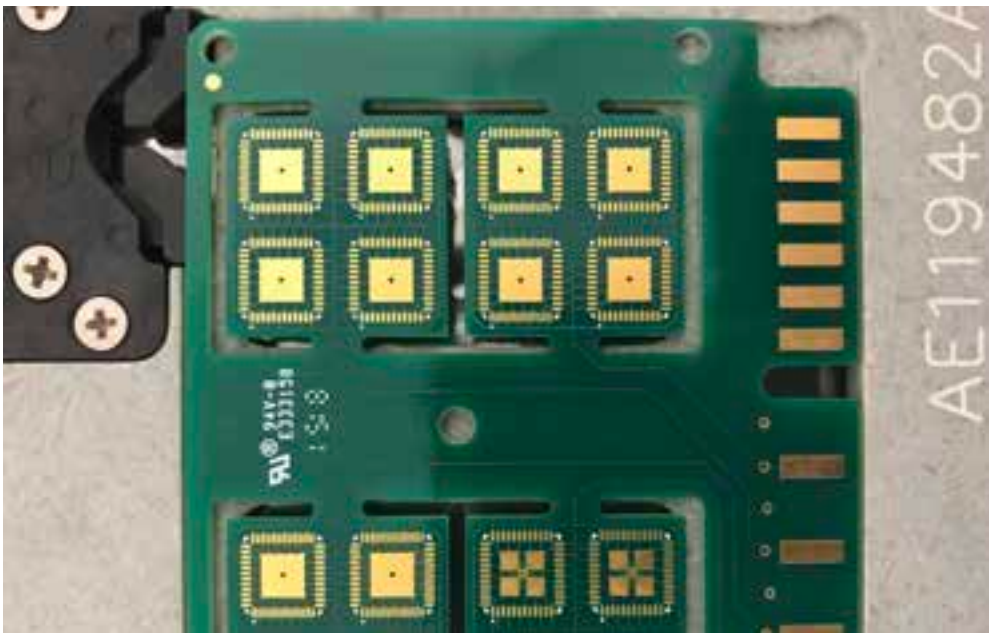

STI QFN TEST VEHICLE - 48 PIN QFN NON DAISY CHAINED PART FOOT PRINT

Figure 1: STI SIR QFN TEST COUPON - SIR Testing of SMT Processing of QFN Components No Clean Flux Chemistry vs. ROL0 Cleanable Chemistry

BY MARK MCMEEN

The electronics industry is facing changing times and how best to define cleanliness and electronic reliability as it relates to overall electronic assembly cleanliness. There are a number of challenges facing the OEM and how best to validate and verify an electronic assembly is clean enough. Which brings up the question of how clean is clean? What's really needed is objective evidence that can be used to ensure electronic hardware is clean enough to meet end customer reliability and warranty objectives. Everybody has looked hard at flux residues and flux chemistry and even thought about component cleanliness, but have you tested your incoming PCBs for ionic contamination? The OEM/contract assembly shops that have to meet certain industry cleanliness expectations such as medical, military and aerospace understand that they must clean/ wash their electronic hardware to meet the end user criticality or warranty and or long term reliability specifications. Particular attention is paid to cleaning underneath Quad Flat No-Lead (QFN), Land Grid Array (LGA) and chip scale packages (CSP) which can be challenging due to their low z axis standoff height and their fine pitch high pin counts. PCB cleanliness is the last thing on OEM/contract electronic assembly companies' mind because the idea of

prewashing incoming boards is not an industry practice. STI Electronics Engineering Lab decided to run a test on bare board suppliers on a STI SIR (Surface Insulation Resistance) Test coupon to see if boards meet the SIR test as an incoming received sample straight out of the package. The test vehicle (Figure 1) was used and two PCB facilities were tested using a standard 48 pin QFN center ground lug component package foot print. The I/O pins are used as SIR sensor traces which allows one to test for surface insulation resistance between adjacent I/O pins and also the center ground lug to see if the component pattern has any plating salts or PCB handling residues or processing Ionics on the surface of component layout/foot print.

The results from running this STI SIR Test coupon were quite interesting: Clean boards saw results of 2E9th to 1E11th while dirty boards saw 5E7th to 3E8th - i.e. Lots of variability in the as received state. The natural pass/fail criteria is 1E8th whereby anything above 1E8th is passing and anything below 9.99E7th is failing. In view of our findings and how once the boards are washed and the results jump to above 5E10th to 9.8E11th for all locations it is easy to discern that PCBs are not clean as an industry standard. The above SIR Test coupon is run 40 degrees C and 90% RH to ensure the board surface has at least 3 to 5 mono layers of water present on the surface of the board which ensures ionic mobility and the test is 168 hours in duration. The above test was initially designed as a mini DOE to discern PCB BASE LINE surface insulation resistance levels for a bare board as received by STI. This mini DOE shows that not all PCB suppliers deliver ionic free or low ionic level PCB cards that are ready for production that meet the SIR level of cleanliness for production builds. The combination of residual plating bath salts and flux residues that have not been fully catalyzed creates an unfavorable ionic mix. When this mix is trapped under a low standoff device, it can very easily create an electrolyte cell that can result in an SIR failure under the device. Over the coming months there will be further studies and insights on PCB cleanliness levels and how best to categorize their risk. Do you know your PCB cleanliness level – SIR value? Should this become a new cleanliness definition? Just a thought…….. The real challenge lies in quantifying cleanliness and their sources and how best to discern and quantify how clean is clean enough?

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if you have any comments or questions concerning this mini DOE.

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