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Planar Micro-Voiding

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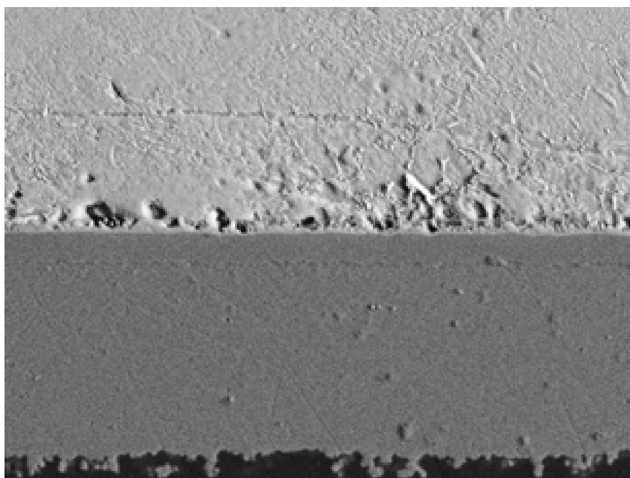
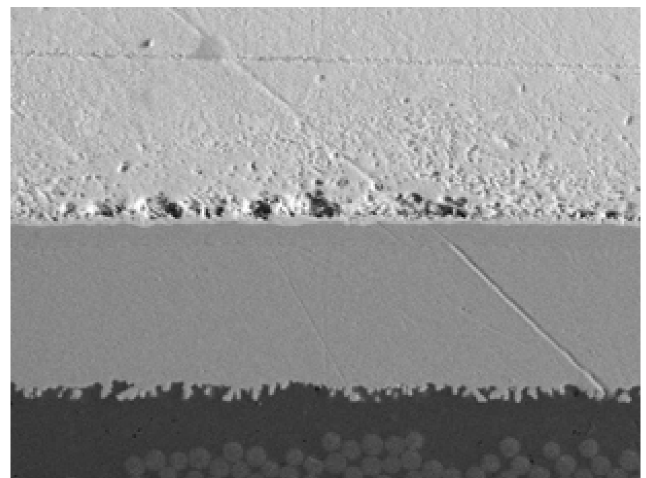
What is planar micro-voiding and why is it a reliability risk? Planar micro-voiding occurs along the intermetallic compound layer (IMC), typically at the PCB pad interface. They are observed to be very small voids (<25 μm) along the topside of IMC layer. Planar micro-voids, however, differ from IMC micro-voids in their location. Planar micro-voids are found at the land-to-solder joint interface whereas IMC micro-voids are found within the IMC or between the IMC and the nickel barrier on electroless nickel immersion gold (ENIG) finished printed circuit boards. The presence of planar micro-voids can lead to areas of the IMC that are insufficient or inconsistent and subject to micro-fracturing and thus reliability related issues. This allows for the IMC, which is already the weakest link and interface within an electrical solder joint or interconnection, to become even weaker and negatively impact long term reliability.

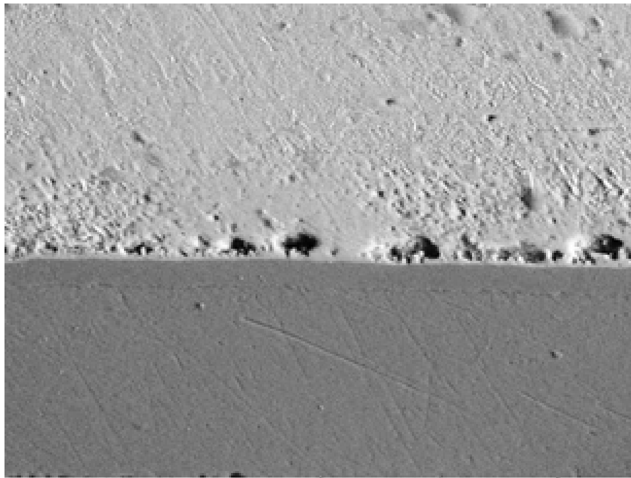
Currently, there is not a lot known in the industry on the root cause of planar micro-voids. It is believed to be a PCB plating issue, with variability seen from lot to lot – process control of the plating bath on a lot to lot basis. In some instances, a correlation has been observed between planar micro-voids and plating process control anomalies. However, this is not always the case and sometimes more

than one underlying issue can lead to the formation of these planar micro-voids, meaning the approach to mitigating the problem can be a multi-step or multi-variable solution. Analytical techniques are often used to help determine what could be the specific issues occurring on the PCB. This can include ionic contamination testing, XRF testing to evaluate the plating thicknesses, and an internal evaluation of the board through cross-sectioning and Scanning Electron Microscope (SEM) imaging. Solutions to try and reduce the presence of planar micro-voiding can include, but are not limited to, pre-cleaning the bare boards to remove any surface contamination that may be present, adjusting the reflow profile to aid in outgassing of volatiles with a longer dwell time in liquidous state, or changing the paste type or paste manufacturer to a more aggressive flux . Research is ongoing to better understand the science behind planer micro-voiding and mitigating this issue going forward.

One hypothesis is the organic brighteners and chemical temperature stabilizer within the plating baths used in the electroless nickel or immersion gold bath is being released and concentrating along the intermetallic formation. These organic chemistries are outgassing during the intermetallic formation stage of the tin / nickel intermetallic and thus are creating this micro-voiding condition. More work is being done on this hypothesis in hopes of finding the root cause. Right now it is found as a potential reliability risk on a lot to lot basis or within a lot itself. Please see the following pictures for a visual aid in the location and size of the planar micro-voiding. Note some planar micro-voiding and IMC micro-voiding could be created by the same source since IMC growth inhibition could be caused by the same outgassing chemistries and thus the source of the problem may be interrelated. More to come as we dive deeper into this problem facing the industry.







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HV: 30.0 kV DATE: 06/08/20 STI Electronics Inc.
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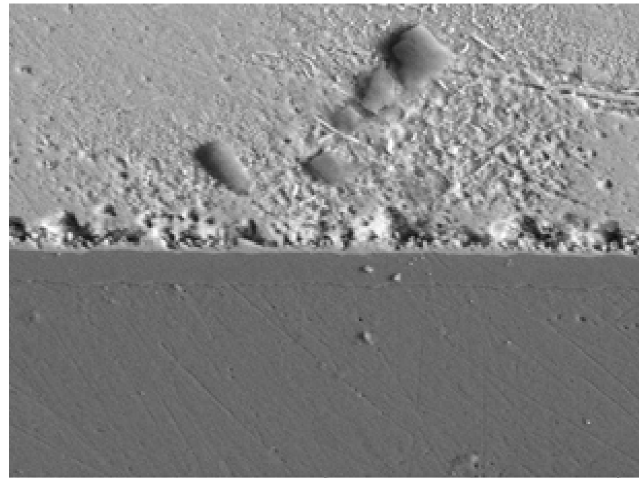

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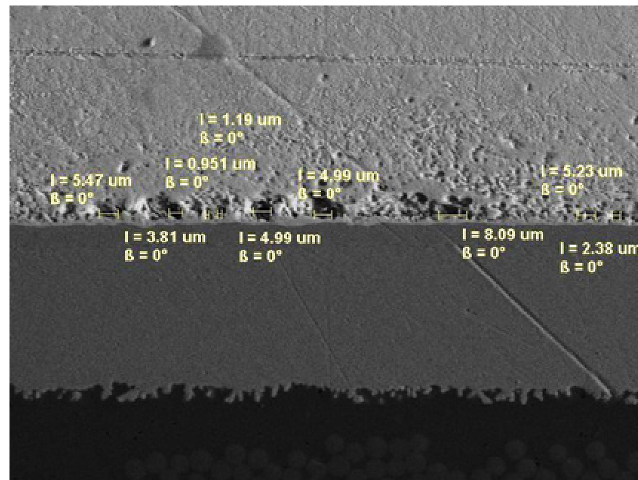

SEM MAG: 2.70 kx DET: BE Detector 50 um Vega ©Tescan
HV: 30.0 kV DATE: 06/08/20 STI Electronics Inc.
VAC: HiVac Device: MV2300VP

If you have any questions or comments please feel free to call or email

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