Can Thermal Cycle Testing be incorporated into SIR Testing to accelerate the test results to find Cleanliness Issues and Weaknesses in Electronic Assemblies?

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STI Electronics and Kyzen Corp. have started to experiment and study the ability to accelerate a multi variable test protocol that looks at that question. Thermal cycling has been around and has a long history of testing solder interconnection reliability in electronic hardware. The hot to cold cycling is a great acceleration test protocol used to look for poor solderability and solder interconnection issues. Coefficient of thermal expansion (CTE) stress is the failure mechanism that accelerates the failure mode if the solder joint / interconnection is suspect or has been processed / soldered incorrectly. This proven technique is good at finding weaknesses in material choices and or processing issues of leaded and unleaded solder alloys.

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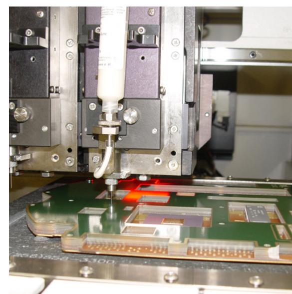
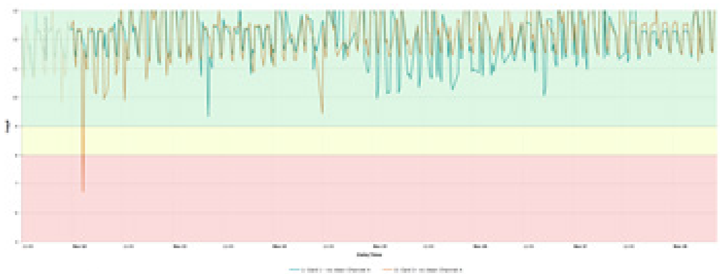


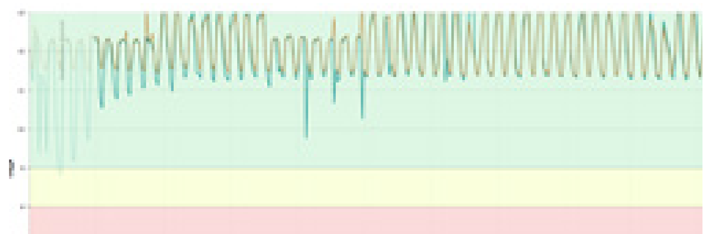
Can the same concept be applied to an SIR test with temperature cycling to help accelerate the test to help find weaknesses in cleanliness underneath components – ie. bottom terminated components which are susceptible to unactivated flux residues. The ability to thermal cycle during SIR testing introduces a new failure mechanism of frost and condensation as it cycles between -40c and 40c. The following test protocol was used whereby test cards were run to accelerate both thermal cycling -40 to 40 with SIR measurements to see if we can detect issues. Note these test vehicles passed standard SIR pre and post thermal cycle testing in the 10 to 11 log ohm range. Note the failure spikes.

This is a QFN with no thermal vias in the ground lug region - thus minimal ingression / access underneath the QFN device

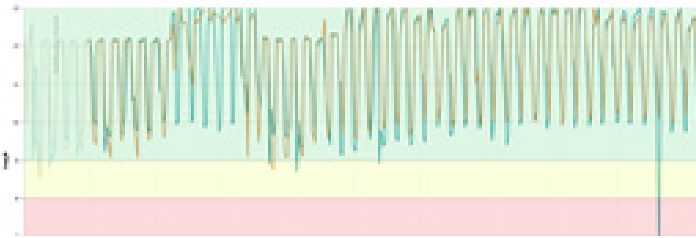
NO CLEAN



2 FPM CLEAN

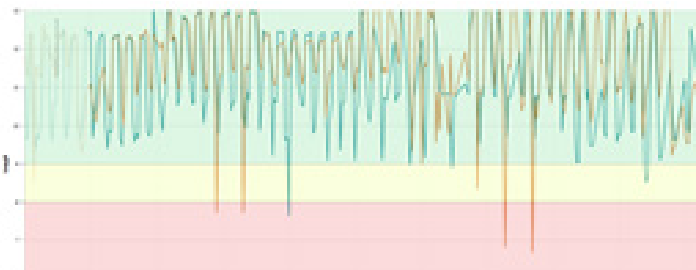


.5 FPM CLEAN

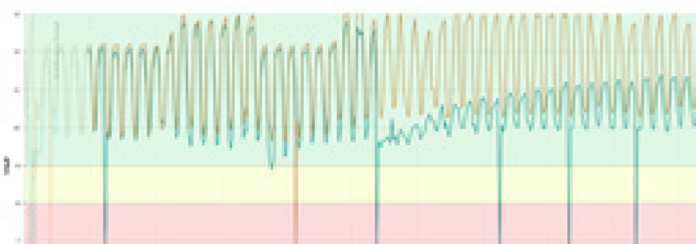


This is a QFN with thermal vias in the ground lug region - this has numerous ingression access points underneath the QFN device

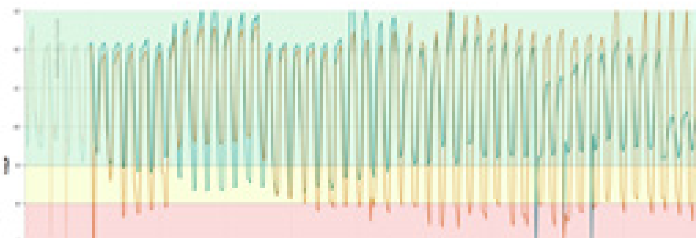
NO CLEAN - NOTE THE SPIKES AND SHORT



2FPM CLEAN – NOTE THE SPIKE INTO RED REGION



.5FPM CLEAN - NOTE THE SPIKES INTO RED REGION



CONCLUSION:

Even though these test vehicles passed standard SIR TEST PROTOCOL OF 40 / 90% RH pre and post Thermal Cycle testing with SIR testing the actual thermal cycle test protocol with SIR measurements found an interesting pcb design issue. The ability to have a thermal via void region underneath the Bottom Terminated Component (BTC) allowed for moisture ingression and accumulation of ionics to a level whereby leak currents could occur and thus manifest in downward spikes as measured by SIR. The non- thermal via designed pcb test vehicle for QFN component style performed better than the design which had thermal vias. This type of testing of using a multivariable acceleration of both thermal cycling and SIR measurement allowed the design team to find a potential root cause mechanism for pcb which would be exposed to environments whereby frost and condensation could occur. Most pcb designers would prefer to design with thermal vias underneath the ground lug region to aid in out gassing of the flux residues underneath BTC components, but in this case whereby this finished electronic assembly would be exposed to environmental extremes of both frost and condensation in its fielded state would not be the preferred pcb design. This also showed that once you cleaned the BTC – QFN part then underfilling it would be beneficial to its long term reliability by eliminating the voided area between the ground lug and signal pins as well as the pin to pin thus eliminating the region whereby free ionics can accumulate and influence your cleanliness state / sir values.

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SUMMARY:

The use of temperature cyclic with condensation is a unique test tool and protocol that is designed to put a number of variables into an accelerated format to find and uncover weaknesses in electronic assembly methods. This test is designed to find cleanliness issues as well as design issues and manufacturing process issues.

By using this multi variable test that uses both hot and cold thermal cycling to drive coefficient of thermal expansion (cte) (-40 to 40c) and the introduction of frost and condensation into the test protocol aids in ionic mobility and high humidity. These conditions aids in the dew point condensation and frost condition. This is an extreme accelerated test to uncover and find weaknesses in material choices, process control, process parameters, and circuit card layout design and component package choices.

This Particular test DOE exposed the problem with via structures underneath BTC (Bottom Terminated Components) by crating voids and blank space for frost and condensation to ingress into the area that we needed to be clean and minimize ionic movement and leakage currents. The idea of via structures for improving out gassing and minimizing unvolatized flux residues, which improves SIR results is quite proven as a good design rule. The vulnerability of ingression issues underneath BTC during thermal cyclic environments with frost and condensation shows the need for better test methodologies for design engineers to insure they address these potential failure modes in real fielded applications. This DOE was designed to explore the need to gather real test data and objective evidence to help develop new test protocols that better define BTC vulnerabilities and create a greater understanding of the variables that greatly impact BTC's.

SIR testing along with temperature cyclic testing with frost / condensation is a good tool in collecting beneficial data and objective evidence of what material sets, production parameters, and process control parameters, and design rules and layout best practices to meet your fielded environmental objectives. SIR testing using specific real world components (SIR Designed test components) in a test environment and in different layout designs allows for determining and finding the weakest link in your design and which design gives you the best results from an SIR cleanliness objective before testing it in the final layout configuration. The more testing and objective evidence one can perform at the development and design stage the better the final design will work in a real fielded state because of the lessons learned on the front end.

This DOE showed how SIR test data in a non - thermal cyclic state all passed with sir readings in the Log 10 and 11 range but once thermal cyclic testing with frost and condensation started then downward spikes and a drop in SIR was seen on the different designed pad and via structures. Depending on your fielded application the use of SIR alone and in conjunction with thermal cyclic testing may better prepare and prevent latent warranty issues in production.